dielectric layer of a first thickness d1 having a top layer 206 which exhibits a high resistance to oxidation at high temperatures. In one embodiment, the first transistor having a dielectric layer of a first thickness d1 has a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness d1 of the dielectric layer. In one embodiment, the first transistor 201A further includes a gate 220A, a first source/drain region 221A and a second source drain region 223A. In one embodiment, the second transistor 201B further includes a gate 220B, a first source/drain region 221B and a second source drain region 223B.

Applicant respectfully submits that the amendments to the specification as detailed above are enabled to one skilled in the art. Applicant submits the amendments therefore do not add new matter.

REMARKS

Applicant has carefully reviewed and considered the Office Action dated April 24, 2002, and the references cited therewith.

No claims are amended or cancelled. Claims 33-40 and 55-86 remain pending in this application.

Form 1499

Applicant notes that the Hideo reference as originally submitted by Applicant and listed on the top of sheet 2 of the form 1499 was not initialed as having been considered by the Examiner. Applicant respectfully requests that the Examiner review the Hideo reference and return an initialed form 1499 in the next communication.

§102 Rejection of the Claims

In the Office Action, claims 33 and 34 were rejected under 35 USC § 102(b) as being anticipated by Okazawa (U.S. Patent No. 4,700,212).

The rejection in page 3, paragraph 6 of the pending Office Action states that Okazawa discloses: